Electronic Version
Stylesheet Version v1.1.1

AUTOMATIC BIT FAIL MAPPING FOR EMBEDDED MEMORIES WITH CLOCK MULTIPLIERS

Abstract

A bit fail map circuit accurately generates a bit fail map of an embedded memory such as a DRAM by utilizing a high speed multiplied clock generated from a low-speed Automated Test Equipment (ATE) tester. The circuit communicates between the ATE tester, the embedded memory under test, Built-In Self-Test (BIST) and Built-In Redundancy Analysis (BIRA). An accurate bit fail map of an embedded DRAM memory is provided by pausing the BIST test circuitry at a point when a fail is encountered, namely a mismatch between BIST expected data and the actual data read from the array, and then shifting the bit fail data off the chip using the low-speed ATE tester clock. Thereafter, the high-speed test is resumed from point of fail by again running the BIST using the high-speed internal clock, to provide at-speed bit Fail Maps.